Reading 11

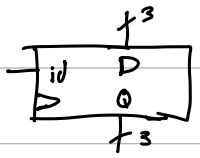
13.3 Load Registers

- A designer may want to load a register only on certain clock cycles rather than on every cycle.

- An N-bit load register stores N bit values.

- All registers in a system typically share the same clock, synchronizing loading of all registers.

- Block Symbol:



- A simpler load-register implementation uses the clock ANDed with the load control line to clock the flip flops, and thus needs no muxes. But gating the clock may lead to unwanted clock skew, where various registers switch output values at slightly different times.

- Synchronous and Asynchronous resets exist.

13.5 Counters and Timers

- A N-bit binary counter is a register whose value increments (+1) or decrements (-1) at each block cycle.

- The counter modulus is $M = 2^N$, usually stated as a decimal value.
  - ↳ The maximum count is $(M-1)$ so $(2^N - 1)$.

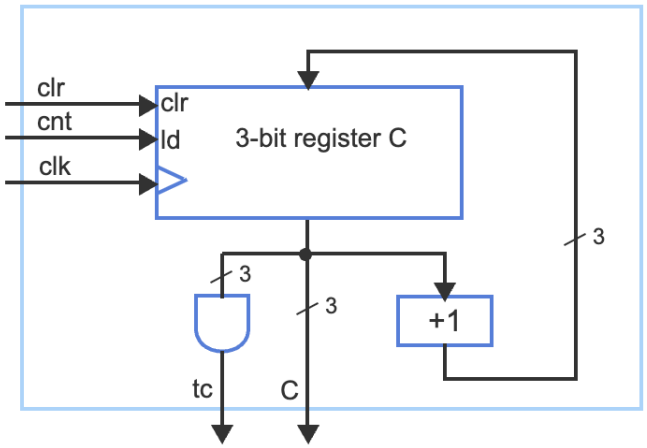
- An up-counter increases the count value by one every clock cycle.

- Upon reaching the highest value, the counter wraps around to 0 and continues counting.

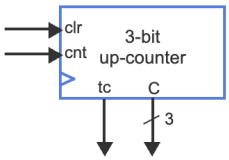
- Most counters include a terminal count (tc) output to indicate the count has reached the last (terminal) value before wrapping around.

- Ripple carry out (rco) or carry out: connecting tc (rco) to the cnt input of another N-bit counter yields a combined 2N-bit counter.

- 3 bit up-counter



Block symbol

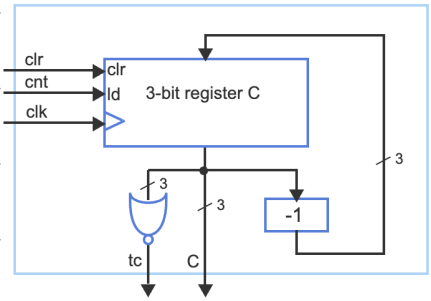


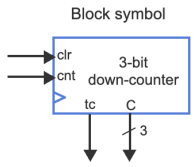
Function table

clr	cnt	Function
0	0	Hold (C = C)
0	1	Count (C ← C + 1)
1	X	Reset (C = 000)

- A N-bit down-counter decreases the counter's stored value by one every clock cycle.
  - ↳ terminal count is 1, when the count is 0, after which the counter's value wraps around to the highest N-bit value.
  - ↳ It resembles an up counter but uses:
    1. a decrementer, not an incrementer
    2. a NOR gate, not an AND, for tc (terminal count) to detect C = 0.

- 3 bit down counter:



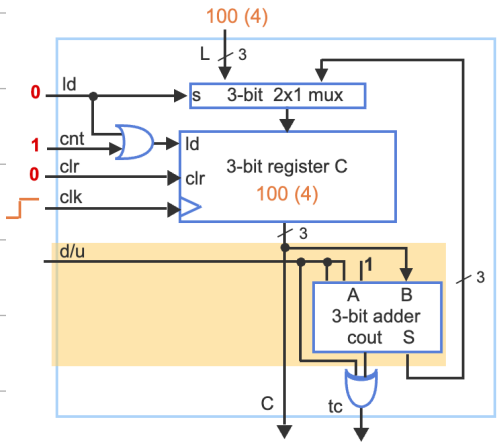


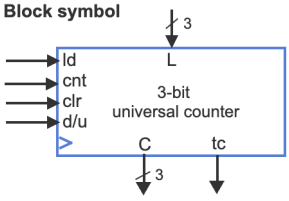
Function table

clr	cnt	Function
0	0	Hold (C = C)
0	1	Count (C ← C - 1)
1	X	Reset (C = 111)

- A presettable counter has an N-bit wide load data input to set the starting value of the count.

- Commercially available counter chips include universal counters: presettable, up/down counters, which can count in both directions. An input called D/U (down/up) or dir chooses the direction, and the tc output may be called min/max.





Function table

clr	ld	cnt	d/u	Function
0	0	0	X	Hold (C = C)
0	0	1	0	Count up (C = C + 1)
0	0	1	1	Count down (C = C - 1)
0	1	X	X	Load (C = L)
1	X	X	X	Reset (C = 000)

- The term **timer** can refer to up-counter or down-counter where the count is a time in seconds (and possibly minutes or hours)

- Combining a presettable down-counter plus a register produces an **interval timer**, a device that generates a 1-clock pulse at a presettable time interval.
  - ↳ The timer's clock period, or base timer unit, is T seconds.

- A timer's **bitwidth** (or width) N determines the maximum possible time interval.
  - ↳ Ex An 8-bit timer with T = 10 μs has a maximum interval P = $2^N \times T = 2^8 \times 10\,\mu s = 2.56$ ms

- 8 bit interval timer with T = 1 μs, pulsing every 50 μs.